WHAT IS CLAIMED IS:

1. An electrically erasable programmable read only memory (EEPROM) cell, comprising:

an isolation layer formed at a semiconductor substrate to define an active region;

a source region, a buried N+ region and a drain region formed at the active region and spaced apart from each other;

a cell depletion region formed at the active region between the buried N+ region and the drain region, the buried N+ region being in contact with the cell depletion region;

a first channel region between the source region and the buried N+ region;

a second channel region between the cell depletion region and the drain region;

a memory gate formed over the first channel region and the buried N+ region;

a selection gate formed over the second channel region; and

a tunnel oxide layer formed on the buried N+ region, wherein distances between the edges of the tunnel oxide layer and the buried N+ region are equidistant.

2. The EEPROM cell of claim 1, wherein the memory gate comprises:

a floating gate;

an inter-gate dielectric layer on the floating gate; and

a control gate electrode on the inter-gate dielectric layer.

3. The EEPROM cell of claim 1, wherein the selection gate comprises:

a lower selection gate;

an inter-gate dielectric layer on the lower selection gate; and

an upper selection gate on the inter-gate dielectric layer, the upper selection gate being electrically connected to the lower selection gate.

4. A method of fabricating an electrically erasable programmable read only memory (EEPROM) cell, comprising the steps of:

forming an isolation layer on a semiconductor substrate to define an active region;

forming a gate oxide layer on the active region;

forming a mask pattern on the gate oxide layer, the mask pattern having an opening that exposes a portion of the gate oxide layer;

implanting impurity ions into the active region using the mask

pattern as an ion implantation mask, thereby forming a buried N+ region in the active region;

forming a spacer pattern on a sidewall of the opening to define a tunnel region surrounded by the spacer pattern;

etching the gate oxide layer in the tunnel region using the mask pattern and the spacer pattern as etching masks, thereby exposing the buried N+ region;

removing the mask pattern and the spacer pattern;

forming a tunnel oxide layer on the buried N+ region in the tunnel region; and

simultaneously forming a memory gate over the buried N+ region and a selection gate spaced apart from the memory gate.

5. The method of claim 4, further comprises implanting impurity ions into the semiconductor substrate using the memory gate and the selection gate as ion implantation masks, thereby forming a source region, a cell depletion region and a drain region, wherein the cell depletion region is formed at the active region between the memory gate and the selection gate to connect with the buried N+ region, the source region is formed to be adjacent to the memory gate and opposite the cell depletion region, and the drain region is formed to be adjacent to the selection gate and opposite the cell depletion region.

6. The method of claim 4, wherein the mask pattern and the spacer pattern are formed of a silicon nitride layer.

7. The method of claim 4, wherein etching the gate oxide layer in the tunnel region is performed using a wet etching technique.

8. The method of claim 4, wherein forming the tunnel oxide layer comprises the steps of:

oxidizing the substrate using an oxygen gas as an ambient gas; and

oxidizing the substrate using a NO gas or a N_2O gas as an ambient gas.

9. A method of fabricating a self-aligned tunnel region in an electrically erasable programmable read only memory (EEPROM) cell, comprising the steps of:

forming a gate oxide layer on an active region of a semiconductor substrate;

forming a mask pattern having predetermined areas that expose portions of the gate oxide layer;

implanting impurity ions into the active region using the mask pattern as an ion implantation mask to form buried N+ regions;

conformally forming a spacer insulating layer on the semiconductor substrate having the buried N+ regions;

anisotropically etching the spacer insulating layer to form spacer patterns on sidewalls of the predetermined areas to define tunnel regions above the buried N+ regions;

etching the gate oxide layer using the mask pattern and the spacer patterns as etching masks to expose the buried N+ region in the tunnel regions;

removing the mask pattern and the spacer pattern; and

forming a tunnel oxide layer on the exposed buried N+ regions in the tunnel regions.

10. The method of claim 9, wherein the mask pattern and the spacer pattern are formed of a silicon nitride layer.

11. The method of claim 9, wherein etching the gate oxide layer in the tunnel region is performed using a wet etching technique.

12. The method of claim 9, wherein forming the tunnel oxide layer comprises the steps of:

oxidizing the substrate using an oxygen gas as an ambient gas; and

oxidizing the substrate using a NO gas or a N_2O gas as an ambient gas.

13. The method of claim 9, further comprising simultaneously forming a memory gate over the buried N+ region and a selection gate spaced apart from the memory gate.

14. The method of claim 13, further comprising implanting impurity ions into the semiconductor substrate using the memory gate and the selection gate as ion implantation masks, thereby forming a source region, a cell depletion region and a drain region, wherein the cell depletion region is formed at the active region between the memory gate and the selection gate to connect with the buried N+ region, the source region is formed to be adjacent to the memory gate and opposite the cell depletion region, and the drain region is formed to be adjacent to the selection gate and opposite the cell depletion region.